EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	42	703/14.ccls. and @pd>"20070501"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/07/16 15:20

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	12	ioput	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/07/16 15:35
L3	71	(bidirectional adj node)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/07/16 15:42
L4	3	(((mixed near signal) or mixed-signal) near simulation) and @pd>"20070501"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/07/16 15:43
L5	0	(((analog near digital) or analog-digital or digital-analog) near simulation) and @pd>"20070501"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/07/16 15:44

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ioput 1900 - 2000 Search Ad Sc Sc

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M Samatham
G Niemeyer
D Hanna
L Svensson
P Enjeti

Did you mean: ***input***

Voltage level translation for an output driver system with a bias generator - all 2 versions »
F Hinedi, M Cases, S Dutta, RH Dennard - US Patent 5,986,472, 1999 - Google Patents
... A gate of transistor 118 is connected to bias circuit 130 at Node E. Adrain of transistor 118 is connected to an information node **IOPUT**, which is connected to ...
Cited by 7 - Related Articles - Web Search

Stacked PFET off-chip driver with a latch bias generator for overvoltage protection - all 3 versions »
F Hinedi, L Mamileti - US Patent 6,141,200, 2000 - Google Patents
... GND **IOPUT** Page 2. ... multiply/add operations, and includes floatingpoint registers output terminal **IOPUT**. 120 performs single precision and/or double precision ...
Related Articles - Web Search

Discrete adaptive control: A sufficient condition for stability and applications - all 3 versions »
JJ Fuchs - Automatic Control, IEEE Transactions on, 1980 - ieeexplore.ieee.org
... we-**ioput** singleootpnt systems is conddered ming a model-reference type appro&. A sufficient condition upon the adaptation naechsnism is obtained Any ...
Cited by 5 - Related Articles - Web Search

Concurrent Hierarchical and Multilevel Simulation of VLSI Circuits - all 3 versions »
RB Mueller-Thuns, JT Rahmeh, JA Abraham, JA Wehbeh ... - SIMULATION, 1993 - intl-sim.sagepub.com
Page 1. 79 TECHNICAL ARTICLE Concurrent Hierarchical and Multilevel Simulation of VLSI Circuits † Robert B. Mueller-Thuns Cadence Design System Inc. ...
Related Articles - View as HTML - Web Search - BL Direct

Circuit and method for voltage level translation utilizing a bias generator - all 2 versions »
F Hinedi, M Cases, S Dutta, RH Dennard - US Patent 5,867,010, 1999 - Google Patents
... the art. Resistor 110 couples clamp device 102 to an external signalling device via signal pad input, **IOPUT**, 112. Diode devices ...
Cited by 4 - Related Articles - Web Search

The de Bruijn multiprocessor network: a versatile parallel processing and sorting network for VLSI - all 9 versions »
MR Samatham, DK Pradhan - IEEE Transactions on Computers, 1989 - doi.ieeecomputersociety.org
... input/sequential output, 2) parallel input/sequential output, 3) parallel inputtharallel output, 4) sequential input&parallel out- put, 5) hybrid **ioput**/l@rid ...
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ioput analog 1900 - 2000 Search Ad Sc Sc

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All Results

R Chadha
T Nguyen
M Steyaert
A Alleyne
C Chen

Did you mean: ***input*** analog

Time-reversal nonlinear emphasis applied to **analog** HDVCR - all 4 versions »
M Kobayashi, A Takeuchi, A Ochi, M Yoneyama, Y ... - Consumer Electronics, IEEE Transactions on, 1992 - ieeexplore.ieee.org
... Time—Reversal Nonlinear Emphasis Fi g 3 Output Waveform of Emphasis Circuit by **analog**
circuits , would ... 2A shows a wave- form of an **ioput** video signal, and Fig ...
Cited by 1 - Related Articles - Web Search - BL Direct

Design methodology and simulation tools for mixed **analog**-digitalintegrated circuits
R Beale, R Chadha, CF Chen, A Prosser, KM Tham - Circuits and Systems, 1990., IEEE International Symposium on, 1990 - ieeexplore.ieee.org
Page 1 Design Methodology and Simulation Tools for Mixed **Analog**-Digital Entegrated Circuits CH2868-8/90/OOOI$I() © 1990 IEEE Richard Beale, Rakesh Chadha, Chin ...
Cited by 1 - Related Articles - Web Search

A semiflash A/D ultra-fast conversion technique
ASC de Menezes, OV de Avilez Filho - Electrotechnical Conference, 1991. Proceedings., 6th ..., 1991 - ieeexplore.ieee.org
... The final circut got from this technique of entirely **analog** and does not use clack ...
For this, we consi dared a current pulse for the unknown **ioput** I, with I25ns ...
Cited by 1 - Related Articles - Web Search

A SIMPLIFIED ALGORITHM FOR DIGITAL DISTANCE PROTECTION BASED ON FOURIER TECHNIQUES - all 3 versions »
DD'Amore, A Ferrero - IEEE Transactions on Power Delivery, 1989 - ieeexplore.ieee.org
... An error reduction as well as a speed increase can be ashieved employing an **analog** band—pass filter on the input signals, in order to cut off the exponential ...
Cited by 5 - Related Articles - Web Search

Integrated communication radio navigation and identification system (ICRNI) - all 3 versions »
J Sinay - Aerospace and Electronics Conference, 1990. NAECON 1990., ..., 1990 - ieeexplore.ieee.org
... equipment. It also isplements algorithms and performs calculations required by other avionics systems and drives the **analog** displays. ...
Web Search

Multilevel verification of MOS circuits - all 3 versions »
D Weise - Computer-Aided Design of Integrated Circuits and Systems, ..., 1990 - ieeexplore.ieee.org
... the schematic of an MOS VLSI circuit, declarations of the logical relationships between the **ioput** signals, aod a ... Circuit components operate on **analog** signals. ...
Cited by 3 - Related Articles - Web Search

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bidirectional node analog 1900 - 2000 Search Ad Sc Sc

Scholar **All articles** - **Recent articles** Results **1** - **10** of about **3,520** for **bidirectional** **node** **analog**. (**0**

All Results
B KOSKO
G Carpenter
N Streitz
B Mukherjee
J Haake

Did you mean: bidirectional ***mode*** analog

Current-mode subthreshold MOS circuits for **analog** VLSI neuralsystems - all 4 versions »
AG Andreou, KA Boahen, PO Pouliquen, A Pavasovic, ... - Neural Networks, IEEE Transactions on, 1991 - ieeexplore.ieee.org
... It is a versatile building block for **analog** signal processing applica- tions designed to ... a current from a high-conductance to a low-conductance **node** (see Fig. ...
Cited by 98 - Related Articles - Web Search

Adaptive **bidirectional** associative memories - all 5 versions »
B KOSKO - Applied Optics, 1987 - OSA
... **bidirectional** associative memory (BAM) behaves as a two-layer hierarchy of symmetrically ... every BAM adaptively resonates in the sense that all **nodes** and edges ...
Cited by 259 - Related Articles - Web Search

SEPIA: a cooperative hypermedia authoring environment - all 10 versions »
N Streitz, J Haake, J Hannemann, A Lemke, W Schuler ... - Proceedings of the ACM conference on Hypertext, 1993 - portal.acm.org
... a digital audio channel for au- dio-only conferencing as well as an **analog** audio/video ... user (eg Haake) at the network level and within WSCRAWL at the **node** level ...
Cited by 220 - Related Articles - Web Search

Fuzzy ART: Fast stable learning and categorization of **analog** patterns by an adaptive resonance ... - all 7 versions »
G Carpenter... - Neural Networks, 1991 - profusion.bu.edu
... it is useful to set fl = 1 when J is an uncommitted **node**, and then ... 1989) described a category proliferation problem that can occur in some **analog** ART systems ...
Cited by 522 - Related Articles - View as HTML - Web Search - Library Search

VLSI architecture for **analog** **bidirectional** pulse-coupled neuralnetworks
Y Ota, BM Wilamowski - Neural Networks, 1997., International Conference on, 1997 - ieeexplore.ieee.org
... Abstract A compact architecture for **analog** CMOS VLSI ... neuron cell is that one **node** serves as ... the neuron cell uses frequency modulated **bidirectional** pulse-streams ...
Cited by 4 - Related Articles - Web Search

Some principles for designing a wide-area WDM optical network - all 4 versions »
B Mukherjee, D Banerjee, S Ramamurthy, A Mukherjee - IEEE/ACM Transactions on Networking (TON), 1996 - portal.acm.org
... that each link in the physical topology is **bidirectional**. ... i), called the physical degree of **node** i. equals ... rates and formars (including some **analog** and some ...
Cited by 177 - Related Articles - Web Search - BL Direct

... /optical access **node** having buffer memory matrix for switchable multi-

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bidirectional "mixed signal" simulation 1900 - 2000 Search Ad Sc Sc

Scholar **All articles** - **Recent articles** Results **1** - **10** of about **192** for **bidirectional** "**mixed signal**" **si**

All Results
S Huynh
S Sunter
S Kim
M Soma
J Zhang

Verilog-AMS: **Mixed-signal simulation** and cross domain connect modules - all 7 versions »
P Frey, DO'Riordan - ... International Workshop on Behavioral Modeling and **Simulation**, 2000 - doi.ieeecs.org
... to-analog converters, or **bidirectional** converters, cause **...** AMS actively supports the **mixed-signal** approach, the **...** were differences in **simulation** semantics between **...**
Cited by 12 - Related Articles - Web Search

Cost/benefit analysis of the P1149. 4 **mixed-signal** test bus - all 3 versions »
SK Sunter, LV Inc, O Ottawa - Circuits, Devices and Systems, IEE Proceedings [see also IEE ..., 1996 - ieeexplore.ieee.org
... factors: the lack of whole chip **simulation** capability the **...** bus Brief description of the PI 149.4 **mixed-signal ...** the pin being an input, output or **bidirectional**. **...**
Cited by 23 - Related Articles - Web Search - BL Direct

Mixed signal integrated circuit architecture and test methodology - all 2 versions »
MB Naglestad, FJ Bohac Jr, JM Aralis, BS Moriwaki, ... - US Patent 5,481,471, 1996 - Google Patents
... designs, including schematic capture, **simulation**, and test **...** comprises aplurality of **mixed-signal** functional blocks. **...** A **bidirectional** digital/analog test bus is **...**
Cited by 14 - Related Articles - Web Search

Evaluating **mixed-signal** simulators - all 2 versions »
D Overhauser, R Saleh - Custom Integrated Circuits Conference, 1995., Proceedings of ..., 1995 - ieeexplore.ieee.org
... analog-to-digital interface, Section IV discusses **bidirectional** interfacing issues **...** involved with H rLuit partitioning for **mixed—signal simulation** and how decis **...**
Cited by 4 - Related Articles - Web Search

[BOOK] Analog Behavioral Modeling with the Verilog-A Languaje - all 3 versions »
D Fitzpatrick, I Miller - 1998 - books.google.com
... mixed-signal components ofthe design is nec- essary for addressing the limited capacity and capabilities oftraditional analog and **mixed-signal simulation** tools **...**
Cited by 34 - Related Articles - Web Search - Library Search

Anatomy of a **simulation** backplane - all 5 versions »
M Zwolinski, C Garagate, Z Mrcarica, TJ Kazmierski ... - Computers and Digital Techniques, IEE Proceedings-, 1995 - ieeexplore.ieee.org
... simplest and most efficient way to develop a **mixed signal simulator** is to **...** 3 Example **simulation** backplane configuration file **...** this global net is **bidirectional**. **...**
Cited by 11 - Related Articles - Web Search

Simulation-based Performance Analysis of Distributed Systems - all 9 versions »
P Schwarz, U Donath - International Workshop Parallel and Distributed Real-Time ..., 1997 -

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IET CNF IET Conference Proceeding

IEEE STD IEEE Standard

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1. **AIDE - A Tool for Computer Architecture Design**
Ellenberger, D.J.; Ng, Y.W.;
Design Automation, 1981. 18th Conference on
29-1 June 1981 Page(s):796 - 803
Abstract | Full Text: PDF(672 KB) IEEE CNF
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2. **On-Line Simulation of Block-Diagram Systems**
Dertouzos, M.L.; Kaliski, M.E.; Polzen, K.P.;
Computers, IEEE Transactions on
Volume C-18, Issue 4, April 1969 Page(s):333 - 342
Abstract | Full Text: PDF(2008 KB) IEEE JNL
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3. **The Open Channel**
Burkhardt, W.H.; Yuen, C.K.;
Computer
Volume 17, Issue 9, Sept. 1984 Page(s):119 - 120
Abstract | Full Text: PDF(2136 KB) IEEE JNL
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4. **Implementation of a fast digital proc essor using the residue number system**
Chao Huang; Peterson, D.; Rauch, H.; Teague, J.; Fraser, D.;
Circuits and Systems, IEEE Transactions on
Volume 28, Issue 1, Jan 1981 Page(s):32 - 38
Abstract | Full Text: PDF(992 KB) IEEE JNL
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5. **On cross coupling and stability in nonlinear control systems**
Rootenberg, J.; Oso, J.;
Automatic Control, IEEE Transactions on
Volume 16, Issue 1, Feb 1971 Page(s):73 - 75
Abstract | Full Text: PDF(344 KB) IEEE JNL
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1. **AQUARIUS: Logic Simulation on an Engineering Workstation**
Sangster, A.; Monahan, J.;
Design Automation, 1983. 20th Conference on
27-29 June 1983 Page(s):93 - 99
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2. **Calculating the effective pattern rate for high-speed board test applications**
Arena, J.J.;
Industrial Electronics, IEEE Transactions on
Volume 36, Issue 2, May 1989 Page(s):164 - 174
Digital Object Identifier 10.1109/41.19065
AbstractPlus | Full Text: PDF(764 KB) IEEE JNL
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3. **Process control by on-line trained neural controllers**
Tanomaru, J.; Omatu, S.;
Industrial Electronics, IEEE Transactions on
Volume 39, Issue 6, Dec. 1992 Page(s):511 - 521
Digital Object Identifier 10.1109/41.170970
AbstractPlus | Full Text: PDF(896 KB) IEEE JNL
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4. **ORACLE - A Simulator for Bipolar and MOS IC Design**
d'Abreu, M.A.; Cheong, K.L.; Flanagan, C.T.;
Design Automation, 1984. 21st Conference on
25-27 June 1984 Page(s):343 - 349
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   Electronics Letters
   Volume 34, Issue 25, Part Supplement, 10 December 1998 Page(s):2445 - 2490
   AbstractPlus | Full Text: PDF(6048 KB) IET JNL

2. **A CMOS mixed signal simultaneous bidirectional signaling I/O**
   Jackson, S.A.; Blalock, B.J.;
   Circuits and Systems, 1998. Proceedings. 1998 Midwest Symposium on
   9-12 Aug. 1998 Page(s):37 - 40
   Digital Object Identifier 10.1109/MWSCAS.1998.759430
   AbstractPlus | Full Text: PDF(64 KB) IEEE CNF
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   Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Cir
   Regular Papers, IEEE Transactions on]
   Volume 42, Issue 12, Dec. 1995 Page(s):1
   Digital Object Identifier 10.1109/TCSI.1995.481202
   AbstractPlus | Full Text: PDF(2168 KB) IEEE JNL
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4. **Minimum time control of a buck converter by means of fuzzy logic approximation**
   Gomariz, S.; Alarcon, E.; Martinez, J.A.; Poveda, A.; Madrenas, J.; Guinjoan, F.;
   Industrial Electronics Society, 1998. IECON '98. Proceedings of the 24th Annual Conference of the
   Volume 2, 31 Aug.-4 Sept. 1998 Page(s):1060 - 1065 vol.2
   Digital Object Identifier 10.1109/IECON.1998.724242
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   Huynh, S.D.; Seongwon Kim; Soma, M.; Jinyan Zhang;
   Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [see also Circ
   Express Briefs, IEEE Transactions on]
   Volume 46, Issue 5, May 1999 Page(s):565 - 576
   Digital Object Identifier 10.1109/82.769805
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